Claims:

1-14(Canceled).

15(Original). An apparatus comprising:

a plurality of first adders, each first adder of the plurality of first adders operative to add two operands of a plurality of operands into one of a plurality of intermediate results;

a plurality of second adders, each second adder of the plurality of second adders operative to add two intermediate results of the plurality of intermediate results into one of a plurality of sum results; and

discard circuitry operative to discard the two least significant bits of each sum result of the plurality of sum results.

16(Original). The apparatus as recited in Claim 15, wherein the plurality of first adders comprises eight first adders and the plurality of second adders comprises seven second adders.

17(Original). The apparatus as recited in Claim 15, wherein the discard circuitry comprises a plurality of shift registers.

18(Original). The apparatus as recited in Claim 15, wherein each of the first adders are operative to add two eight-bit input operands producing a nine-bit intermediate operand and each of the second adders are operative to add two nine-bit intermediate operands producing a ten-bit output operand.

19(Original). The apparatus as recited in Claim 15, wherein each of the first adders are operative to add two sixteen-bit input operands producing a seventeen-bit intermediate operand and each of the second adders are operative to add two seventeen-bit intermediate operands producing an eighteen-bit operand.

20(Original). The apparatus as recited in Claim 15, wherein routing of the plurality of operands and the plurality of intermediate results to the plurality of first adders and the plurality of second adders is selected according to microcode identified by a Single-Instruction/Multiple-Data (SIMD) instruction.

21(Original). The apparatus as recited in Claim 15, wherein routing of the plurality of operands and the plurality of intermediate results to the plurality of first adders and the plurality of second adders is selected according to decode logic and a Single-Instruction/Multiple-Data (SIMD) instruction.

22(Original). The apparatus as recited in Claim 15, wherein the plurality of first adders, the plurality of second adders, and the discard circuitry form a Single-Instruction/Multiple-Data (SIMD) instruction execution circuit.

23-36(Canceled).